TMS
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Control of the DES CCD –
Clock and Clock Rail Sharing Possibilities

This note is meant to document some initial thoughts on what is required to readout a single CCD of the DECam. The production system will contain an array of 62 CCD devices as well as an additional 8 CCDs which will be used to guide and focus the telescope.

The CCD chosen for DECam is a LBL 2Kx4K two channel device. The device is best described by the document "**LBL CCD Operating Procedures**", which can be found at http://www-eng.lbl.gov/~karcher/BI_data.pdf

We make the following assumptions in our intended use of the CCD:

- No Frame Store.
  This means that we tie the frame store clocks (FS1, FS2, FS3) to the vertical clocks (V1, V2, V3). This is done on the AlN board to which the CCD is mounted.
- Dual channel readout will be supported.
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Open decisions:

- Do we need to individually control all Bias/clock level voltages for each CCD or CCD half independently?
  It seems like we should plan on this until we have evidence it is not required. We may have to make this decision before looking at a large number of CCDs.
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The following page contains a figure which shows a top level block diagram of what we need to provide in order to readout a single CCD. It makes no assumptions as to where any of the electronics is located.

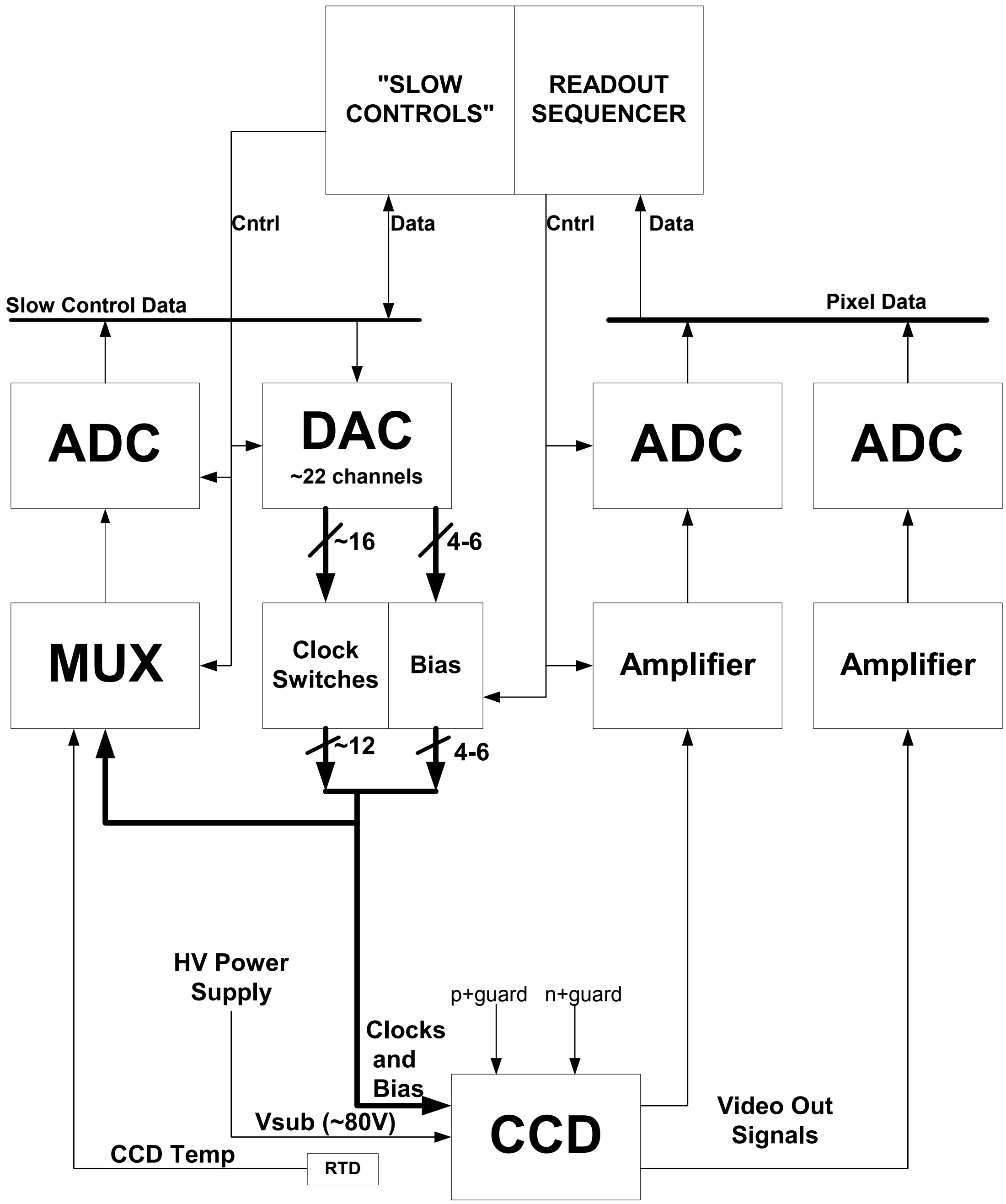

Figure 1. Readout requirements for a single CCD

List of Bias Voltages required by LBL CCD

The following voltage bias rails are required by the LBL CCD:

Signal	**Function**	**Typical value**	**Range**
Vdd	Output Drain	-22V	-25V to 0V
Vr	Reset Drain	-12.5V	-15V to 0V
Vog	Output Gate	2.16V	0 to 5V

Note that there are separate pins for the U and L halves of the CCD. Worst case means that we should plan on providing **six** bias voltages for each CCD. According to Ricardo Schmidt, we can probably safely plan on using a single bias setting for Vdd U/L and Vog U/L. The Reset Drain voltage is best left controllable on each half of the chip so that it can be adjusted for best linearity. This could get us down to **four** independently controlled bias voltages for each CCD.

LBL CCD Guard voltages

There are two guard voltages on the LBL CCD.

The n+ guard is to be left floating; however, one possible erase mechanism calls for the n+ guard to be shorted to ground.

The p+ guard is grounded.

List of Clocks and Clock levels required by LBL CCD

The following table shows a list of the clock signals used by the LBL CCD and their nominal switching levels:

Signal	**Function**	**Typical High/Low Voltage**
V1, V2, V3 FS1, FS2, FS3	Vertical Clocks Frame Store Clocks	+5V / -3V
Tg	Transfer Gate	+5V / -3V
H1, H2, H3	Horizontal Clocks	+6V / -4V
SW	Summing Well	+5V / -5V
Rg	Reset Gate	0V / -6V

Once again, each of these signals has separate pins for the U and L halves of the CCD.

Since we do not plan on using the frame store feature of the device, we can eliminate the need to control the FS1,FS2 and FS3 clock lines. These will be tied to the V1, V2 and V3 lines on the AlN board used to mount the CCD.

Common usage ties the U/L control of the vertical gates (V1,V2, V3 and Tg) together. However, to maintain the flexibility to readout the CCD from both the U and L readout amplifiers, we need to provide separate clocking for the U/L sides of the horizontal clocks (H1, H2, H3, SW and Rg). Ricardo Schmidt further suggests we can group RgU and RgL. I believe we may also be able to provide this logic to SWU and SWL. (ALL THESE ASSUMPTIONS SHOULD BE BENCH TESTED!)

This leaves us with the following **12 clocks we need to control**:
V1, V2, V3, Tg, H1U, H1L, H2U, H2L, H3U, H3L, SW and Rg.

Ricardo Schmidt further suggests that the following rules can be applied to the voltage rails which we use to control these clock levels. We can assume the horizontal clock rails for H1_U, H2_U, H3_U can be shared. Likewise with H1_L, H2_L and H3_L. He suggests we do not make this assumption with the vertical clocks because of the large capacitance each of these lines are driving. If we take this group of assumptions, we come up with the following list of **16 clock rails** we need to provide:

H123U_high	H123U_low
H123L_high	H123L_low
SW_high	SW_low
Rg_high	Rg_low
V1_high	V1_low
V2_high	V2_low
V3_high	V3_low
Tg_high	Tg_low

Question: Can we simplify further, by combining rails for H123_U and H123_L? This would get us down to 14 clock rails.

Question: Can we figure out a way to share V1,V2 and V3 high and low rails by providing local capacitance at switch? This would get us down to 10 clock rails.

Some thoughts on system architecture

Using Monsoon – my summary of email from Ricardo Schmidt (1/14/05)

Ricardo suggests a scheme which will use Monsoon. He suggests that we use two 8-slot Monsoon liquid cooled crates near the Prime Focus cage. He further suggests we run CCDs as pairs (i.e. sharing their clocks and biases). He acknowledges this requires testing at the bench.

With the assumption of 12 clocks, 16 clock rails and 6 bias levels per CCD, we require
12 clocks x 62 CCDs = 744 clocks
16 clock rails x 62 CCDs = 992 clock rails
6 bias levels x 62 CCDs = 372 bias levels
2 video out x 62 CCDs = 124 video outs

with sharing of clocks and bias between 2 CCDs, we have
372 clocks
496 clock rails
186 bias levels
124 video outs

Ricardo suggests a new 16 channel analog board which would also have 24 bias outputs. With 8 such cards we could cover our requirements for handling the video output conversion and the production of the bias levels.

This leaves us 6 slots available for Clock Boards. Each clock board could provide 36 “low voltage biases” to feed the clock rails. This gives us 36 x 6 = 216 clock rails, which would require additional sharing of rails beyond the groupings of 2 CCDs. These clock rails would be driven over to the Vacuum Interface Board (VIB). The VIB would contain clock switches and high impedance buffers.

The Clock Boards also provide 32 “clock outputs”. This would give us a total of 32 x 6 = 192 clock signals. As with the clock voltage rails, additional sharing of these lines would have to occur. These “clock outputs” would basically act as the input to CMOS switches located on the VIB, having nominal swings of 0-5V.

Ricardo points out the following advantages of this system:
1) uses existing Monsoon pieces, other than new 16chanel/24bias Card
2) maintains programmability of all voltage levels with readback

Disadvantages:
Lots of sharing going on of clock rails!

Other thoughts on using Monsoon concept:

Maybe we could redo the Clock Board to better match our requirements?

Maybe we could think of the design of a single new board which would supply clock rails, clocks, biases and analog conversion for 10 channels?

Other Ideas

Some other thoughts involve building small cards which could plug directly into the VIB. These cards would include the analog switches for driving the clock signals as well as the ADCs required for the double correlated sampling. More on this to come……… (complications here include cooling and possibly mechanical support)